The configuration depends on the settings of switches D2850 and D2751. These switches are controlled by the signals FILT, CALDC- HD, SQUAR and Si. Table 3.8 lists the various settings and resulting generator output signals.

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Table 3.8 Generator	COUITOI SIUHAIS	IUI VAIIUUS	ueneraior	uunuun siunais

STII	MUL	L CONTROL SIGNALS		OUTPUT SIGNAL			
frequency	duty cycle	CALDC- HD	FILT	SQUAR	Si	amplitude	waveform
488 Hz	50%	0	0	1	1	5 V p-p	
976 Hz	50%	0	0	1	1	5 V p-p	Square wave voltage
1.95 kHz	50%	0	0	1	1	5 V p-p	
-	-	1	0	0	1	3 V p-p	DC voltage
976 Hz	50%	0	1	0	1	1 V p-p	Sine wave voltage
20 kHz	0-100%	0	1	0	1	-2+2 V p-p	Slow ramp voltage
20 kHz	0-100%	0	1	0	0	0+3 mA	Slow ramp current

In this table "1" means: signal "high" (switch closed) and "0" means signal "low" (switch open).

The slow ramp current signal is made with a current source. A simplified schematic diagram is given in figure 3.17:

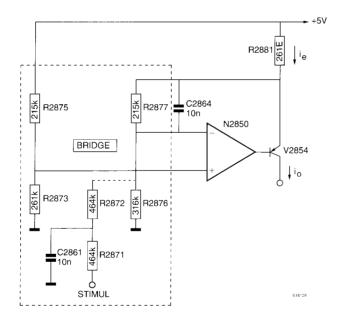


Figure 3.19 Current source section of generator

When the duty cycle of STIMUL is 0%, the bridge will be in balance and current $i_e = 0$. When the duty cycle of STIMUL is increased, a DC component is generated, which has a linear relation to the duty cycle. The operational amplifier tries to keep the voltages on both inputs the same. The operational amplifier will now drive transistor V2854 to increase i_e . Because i_e is almost equal to i_o , the output current will also increase. In this way it is possible to regulate the current i_o by means of the duty cycle of STIMUL.